

JK-mSMD110-33 PPTC DEVICES

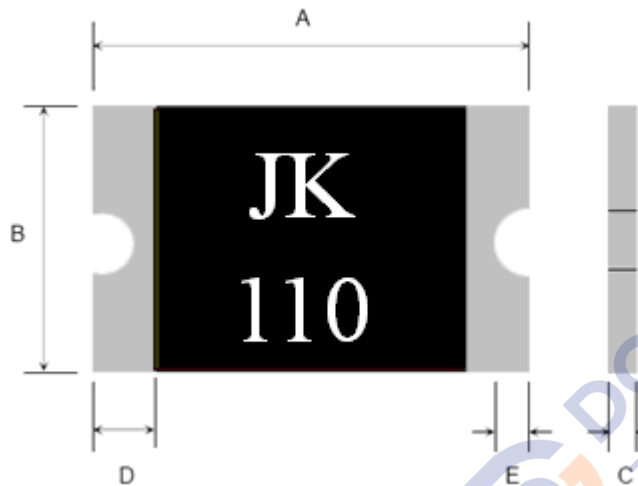
Part Number: Q/JKTD-33-110

Edition: A0

Page No: 1 OF 3



金瑞电子材料  
Jinrui Electronic material



Terminal pad materials :Tin-Plated Nickle-copper

Terminal pad solderability : Meets EIA specification  
RS 186-9E and ANSI/J-STD-002 Category 3.

Marking : JK110=1812(110)

Table1 :DIMENTION(Unit : mm)

Model	Marking	A		B		C		D	E
		Min.	Max.	Min.	Max.	Min.	Max	Min.	Min
JK-mSMD110-33	JK110	4.37	4.73	3.07	3.41	0.90	1.50	0.30	0.25

Table2 :PERFORMANCE RATINGS:

Model	V <sub>max</sub> (Vdc)	I <sub>max</sub> (A)	I <sub>hold</sub> @25℃ (A)	I <sub>trip</sub> @25℃ (A)	P <sub>d</sub> Typ (W)	Maximum Time To Trip		Resistance		
						Current (A)	Time (Sec)	R <sub>i min</sub> (Ω)	R <sub>i typ</sub> (Ω)	R <sub>1 max</sub> (Ω)
JK-mSMD110-33	33	100	1.10	2.20	0.8	8.0	0.30	0.050	0.110	0.280

Table3:Test Conditons and Standards

Item	Test Conditon	Standard
Initial Resistance	25℃	0.050~0.280Ω
I <sub>H</sub>	25℃, 1.10A, 30min	No Trip
Trip	25℃, 8.0A	≤0.30s
Trip endurance	33V, 100A, 1hr	No arcing or burning

Operating Temperature: -40℃ TO 85℃

Packaging: Bulk ,1500pcs per bag

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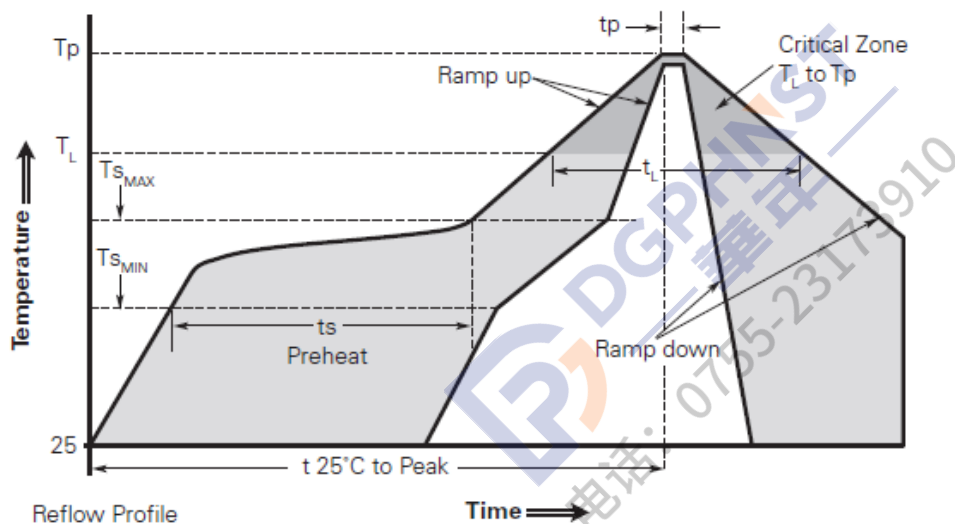
Edition: A0

Page No: 2 OF 3



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Solder reflow conditions



Profile Feature	Pb-Free Assembly
Average ramp up rate (Ts <sub>MAX</sub> to Tp)	3°C/second max.
Preheat	
• Temperature min. (Ts <sub>MIN</sub> )	150°C
• Temperature max. (Ts <sub>MAX</sub> )	200°C
• Time (ts <sub>MIN</sub> to ts <sub>MAX</sub> )	60-120 seconds
Time maintained above:	
• Temperature (T <sub>L</sub> )	217°C
• Time (t <sub>L</sub> )	60-150 seconds
Peak/Classification temperature (Tp)	260°C
Time within 5°C of actual peak temperature	
Time (tp)	30 seconds max.
Ramp down rate	3°C/second max.
Time 25°C to peak temperature	8 minutes max.

**Note:** All temperatures refer to topside of the package, measured on the package body surface.

- Recommended reflow methods: IR, vapor phase oven, hot air oven, N2 environment for lead-free.
- Devices are not designed to be wave soldered to the bottom side of the board.
- Recommended maximum paste thickness is 0.25mm (0.010inch).
- Devices can be cleaned using standard industry methods and solvents.
- Soldering temprature profile meets RoHs leadfree process.

Notes: If reflow temperatures exceed the recommended profile, devices may not meet the performance requirements

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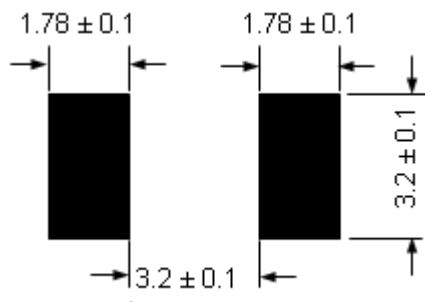
Edition: A0

Page No: 3 OF 3



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## Recommended pad layout (mm)



## WARNING

- Use PPTC beyond the maximum ratings or improper use may result in device damage and possible electrical arcing and flame.
- PPTC are intended for protection against occasional over current or over temperature fault conditions and should not be used when repeated fault conditions or prolonged trip events are anticipated.
- Device performance can be impacted negatively if devices are handled in a manner inconsistent with recommended electronic, thermal, and mechanical procedures for electronic components.
- Use PPTC with a large inductance in circuit will generate a circuit voltage ( $L \frac{di}{dt}$ ) above the rated voltage of the PPTC.
- Avoid impact PPTC device its thermal expansion like placed under pressure or installed in limited space.
- Contamination of the PPTC material with certain silicon based oils or some aggressive solvents can adversely impact the performance of the devices. PPTC SMD can be cleaned by standard methods.
- Requests that customers comply with our recommended solder pad layouts and recommended reflow profile. Improper board layouts or reflow profile could negatively impact solderability performance of our devices.