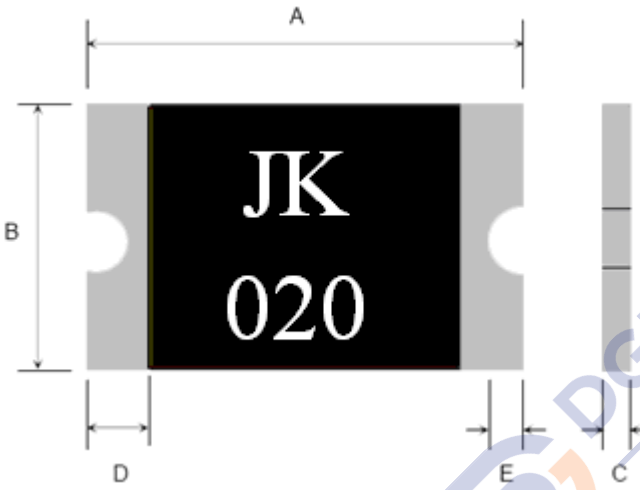
JK-mSMD020 PPTC DEVICES

Part Number: Q/JKTD-60-020

Edition: A0



Terminal pad materials :Tin-Plated Nickle-copper

Terminal pad solderability : Meets EIA specification RS 186-9E and ANSI/J-STD-002 Category 3.

Marking : JK020=1812(020)

Table1 :DIMENTION(Unit : mm)

Model	Marking	A		B		C		D	E
		Min.	Max.	Min.	Max.	Min.	Max	Min.	Min
JK-mSMD020	JK020	4.37	4.73	3.07	3.41	0.50	1.00	0.30	0.25

Table2 :PERFORMANCE RATINGS:

Model	V_{max}	I_{max}	I_{hold} @25℃	I_{trip} @25℃	P_d Typ	Maximum Time To Trip		Resistance		
						Current	Time	Ri_{min}	Ri_{typ}	$R1_{max}$
	(Vdc)	(A)	(A)	(A)	(W)	(A)	(Sec)	(Ω)	(Ω)	(Ω)
JK-mSMD020	60.0	100	0.20	0.40	0.8	8.0	0.02	0.350	0.800	5.000

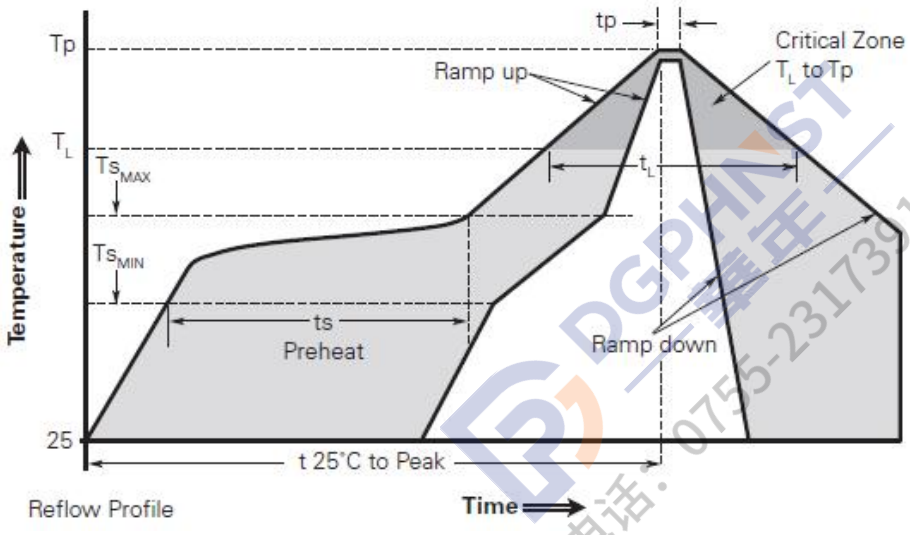
Table3:Test Conditons and Standards

Item	Test Conditon	Standard
Initial Resistance	25℃	0.350～5.000Ω
I_H	25℃，0.20A， 60min	No Trip
Ttrip	25℃，8.0A	≤0.02s
Trip endurance	60V，100A， 1hr	No arcing or burning

Operating Temperature：-40℃ TO 85℃

Packaging：Bulk ,1500 pcs per bag

Solder reflow conditions



Reflow Profile

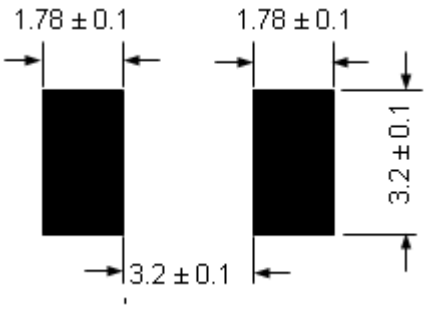
Profile Feature	Pb-Free Assembly
Average ramp up rate (Ts_{MAX} to Tp)	3°C/second max.
Preheat	
• Temperature min. (Ts_{MIN})	150°C
• Temperature max. (Ts_{MAX})	200°C
• Time (ts_{MIN} to ts_{MAX})	60-120 seconds
Time maintained above:	
• Temperature (T_L)	217°C
• Time (t_L)	60-150 seconds
Peak/Classification temperature (Tp)	260°C
Time within 5°C of actual peak temperature	
Time (tp)	30 seconds max.
Ramp down rate	3°C/second max.
Time 25°C to peak temperature	8 minutes max.

Note: All temperatures refer to topside of the package, measured on the package body surface.

- Recommended reflow methods: IR, vapor phase oven, hot air oven, N2 environment for lead-free.
- Devices are not designed to be wave soldered to the bottom side of the board.
- Recommended maximum paste thickness is 0.25mm (0.010inch).
- Devices can be cleaned using standard industry methods and solvents.
- Soldering temprature profile meets RoHs leadfree process.

Notes: If reflow temperatures exceed the recommended profile, devices may not meet the performance requirements

Recommended pad layout (mm)



WARNING

· Use PPTC beyond the maximum ratings or improper use may result in device damage and possible electrical arcing and flame.

· PPTC are intended for protection against occasional over current or over temperature fault conditions and should not be used when repeated fault conditions or prolonged trip events are anticipated.

· Device performance can be impacted negatively if devices are handled in a manner inconsistent with recommended electronic, thermal, and mechanical procedures for electronic components.

· Use PPTC with a large inductance in circuit will generate a circuit voltage (L di/dt) above the rated voltage of the PPTC.

· Avoid impact PPTC device its thermal expansion like placed under pressure or installed in limited space.

· Contamination of the PPTC material with certain silicon based oils or some aggressive solvents can adversely impact the performance of the devices.PPTC SMD can be cleaned by standard methods.

· Requests that customers comply with our recommended solder pad layouts and recommended reflow profile. Improper board layouts or reflow profilecould negatively impact solderability performance of our devices.