Application Note: SY6861A1/A2/B1/B2

5.5V, 3A Low Loss Power Distribution Switch With Reverse Block Rating Up to 28V

General Description

SY6861A1/A2/B1/B2 is an ultra-low $R_{DS(ON)}$, 3A low loss power distribution switch with current limit to protect the power source from over current and short circuit conditions.

SY6861A1/A2/B1/B2 has over voltage protection and the output pin can withstand 28V. It incorporates the over-temperature protection and reverse blocking functions.

Features

- Input Voltage: 2.5V to 5.5V
- Output Voltage Withstanding 28V
- Extremely Low Power Path Resistance: 45mΩ (typ.)
- 3A Load Current Capability
- Reverse Blocking in Normal Operation or Shutdown
- Fault Flag (OCB) Output For Over Current and Fault Conditions
- Compact Package: SOT23-5/SOT23-6
- RoHS Compliant and Halogen Free
- UL Certification NO. E491480

Ordering Information

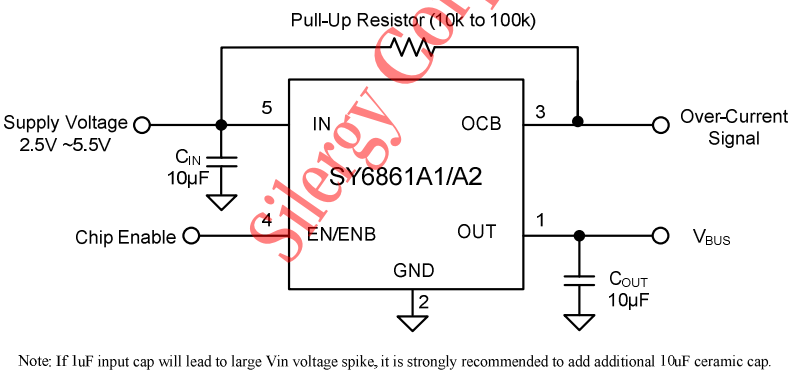
SY6861 □(□□)□
- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package Type	Note
SY6861A1AAC	SOT23-5	Active High
SY6861A2AAC	SOT23-5	Active Low
SY6861B1ABC	SOT23-6	Active High
SY6861B2ABC	SOT23-6	Active Low

Applications

- USB 3.1 Application
- USB 3G Datacard
- USB Dongle
- MiniPCI Accessories
- USB Charger
- Public Place Multi-USB Charger

Typical Applications



Note: If 1uF input cap will lead to large Vin voltage spike, it is strongly recommended to add additional 10uF ceramic cap.

Figure 1. SY6861A1/A2 Schematic Diagram

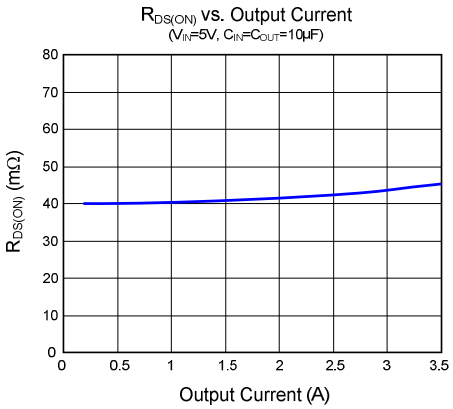
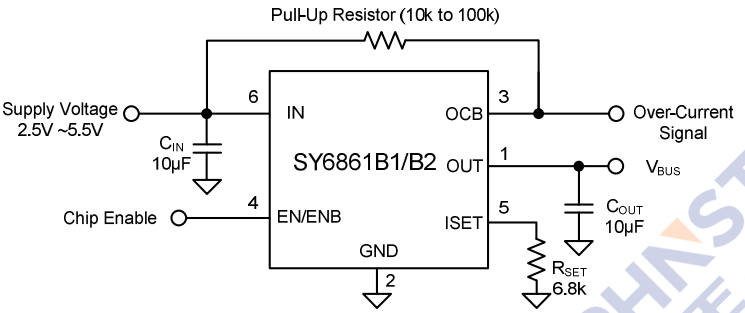


Figure 2. $R_{DS(ON)}$ vs. Output Current



Note: If 1uF input cap will lead to large Vin voltage spike, it is strongly recommended to add additional 10uF ceramic cap.

Figure 3. SY6861B1/B2 Schematic Diagram

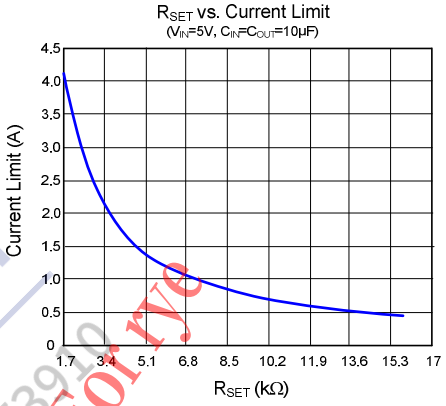
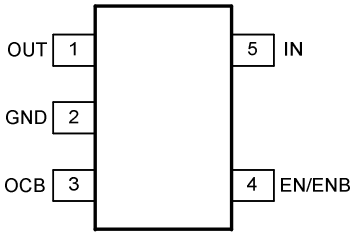
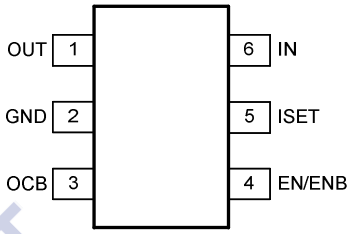


Figure 4. R_{SET} vs. Current Limit

Pinout (top view)



(SOT23-5)



(SOT23-6)

Top Mark: **Td*xyz*** for SY6861A1AAC **(**Device code: Td; ***x=year code, y=week code, z= lot number code*****)**
Vg*xyz* for SY6861A2AAC **(**Device code: Vg; ***x=year code, y=week code, z= lot number code*****)**
Te*xyz* for SY6861B1ABC **(**Device code: Te; ***x=year code, y=week code, z= lot number code*****)**
Vh*xyz* for SY6861B2ABC **(**Device code: Vh; ***x=year code, y=week code, z= lot number code*****)**

Pin Name	Pin number		Pin Description
	SOT23-5	SOT23-6	
OUT	1	1	Output pin.
GND	2	2	Ground pin.
OCB	3	3	Fault Flag. Open drain under normal conditions, grounded under fault operation.
EN/ENB	4	4	ON/OFF control. Do not leave it floating. EN: Active high. ENB: Active low.
IN	5	6	Input pin.
ISET	--	5	Current limit programming pin. Connect a resistor R_{SET} from this pin to ground to program the current limit: I_{LIM} (A)=6800/R_{SET} (Ω)

Block Diagram

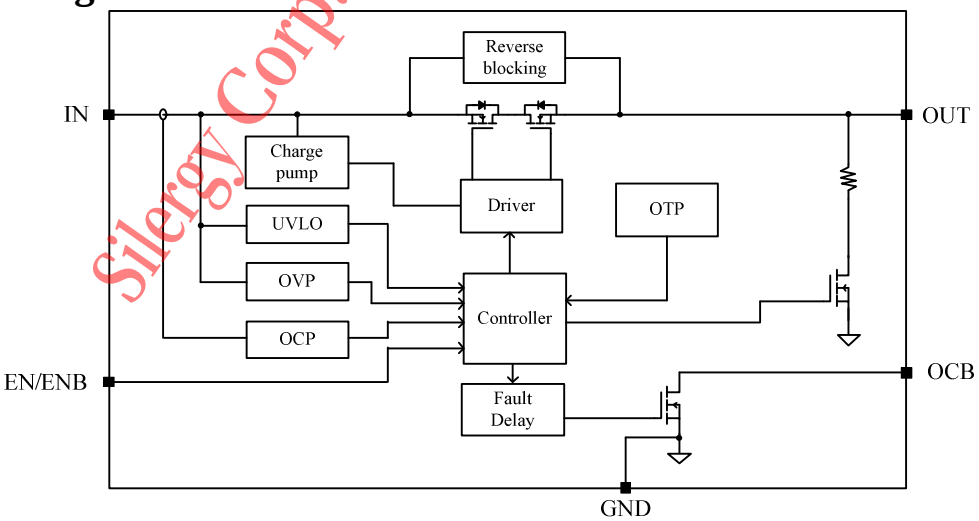


Figure 5. SY6861A1/A2 Block Diagram

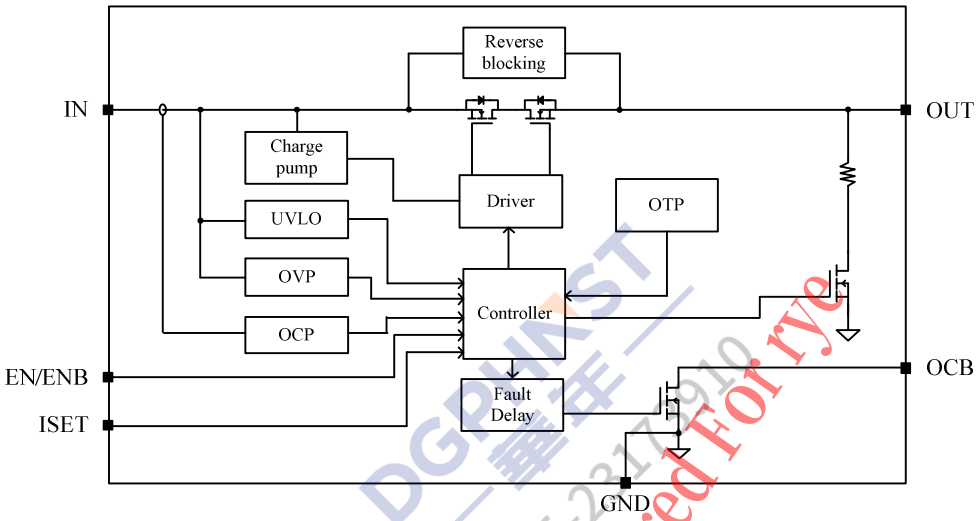


Figure 6. SY6861B1/B2 Block Diagram

Absolute Maximum Ratings (Note 1)

IN ---------- -0.3V to 7V
ISET ---------- -0.3V to 3.6V
OCB, EN, ENB, OUT ---------- -0.3V to 28V
Power Dissipation, P_D @ T_A = 25°C SOT23-5/SOT23-6 ---------- 1.2W/1.2W
Package Thermal Resistance (Note 2)
θ_{JA}, SOT23-5/SOT23-6 ---------- 83°C/W/81°C/W
θ_{JC}, SOT23-5/SOT23-6 ---------- 17°C/W/14°C/W
Junction Temperature ---------- 150°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -65°C to 150°C
ESD Susceptibility
HBM (Human Body Mode) ---------- 2kV
CDM (Charged Device Mode) ---------- 500V

Recommended Operating Conditions (Note 3)

IN ---------- 2.5V to 5.5V
ISET ---------- 0V to 3.3V
All other pins ---------- 0V to 22V
Junction Temperature Range ---------- -40°C to 125°C
Ambient Temperature Range ---------- -40°C to 85°C

Electrical Characteristics

(V_{IN} = 5V, C_{OUT}=10μF, T_A = 25°C unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range		V_{IN}		2.5		5.5	V
Input Over Voltage Protection		V_{OVP}			5.6		V
OVP Hysteresis		V_{OVP_HYS}			0.1		V
Shutdown Input Current		I_{SHDN}	Open load, switch OFF		5	30	μA
			Output grounded, switch OFF		5	30	μA
Quiescent Supply Current		I_Q	Open load, switch ON		65		μA
FET $R_{DS(ON)}$		$R_{DS(ON)}$	V_{IN}=5V, I_{OUT}=0.3A		45	50	mΩ
Current Limit		I_{LIM}	SY6861A1/A2, V_{IN}=5V, V_{OUT}=4.5V	3.2	3.76	4.43	A
			SY6861B1/B2 R_{SET}=1.878k, V_{IN}=5V, V_{OUT}=4.75V	3.0	3.62	4.16	
Programmable Current Limit Range		I_{LIM_RANGE}	SY6861B1/B2	0.4		4	A
EN/ $\overline{EN}$ Threshold	Logic-Low Voltage	V_{IL}				0.4	V
	Logic-High Voltage	V_{IH}		1.0			V
IN UVLO Threshold		$V_{IN,UVLO}$				2.45	V
IN UVLO Hysteresis		$V_{IN,HYS}$			0.1		V
Rise Time		t_{RISE}	V_{IN}=3.3V, R_L=10Ω, C_L=1μF, V_{OUT}=10%~90%V_{IN}	1.0	1.9	3.0	ms
			V_{IN}=5.0V, R_L=10Ω, C_L=1μF, V_{OUT}=10%~90%V_{IN}	1.5	3.0	4.5	ms
OCB Low Resistance		R_{OCB}			125		Ω
OCB Delay Time		t_{OCB_Delay}			15		ms
OUT Shutdown Discharge Resistance		R_{DSG}		90	115	140	Ω
Discharge Time		t_{DSG}			130		ms
Thermal Shutdown Temperature		T_{SD}			150		°C
Thermal Shutdown Hysteresis		T_{HYS}			20		°C

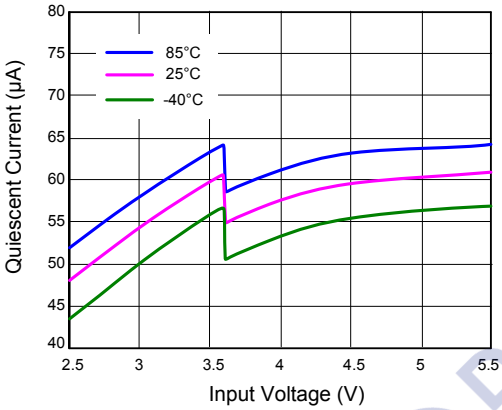
Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a Silergy's test board. Pin 2 of SOT23-5/SOT23-6 package is the case position for θ_{JC} measurement.

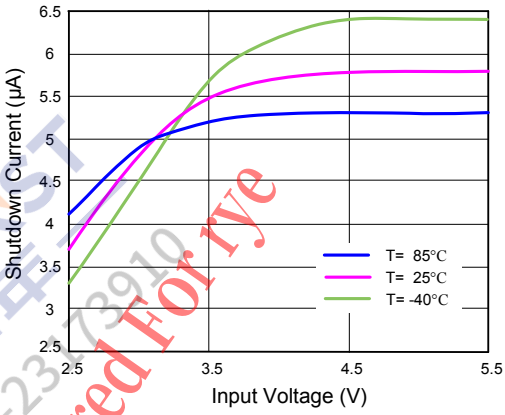
Note 3: The device is not guaranteed to function outside its operating conditions.

Typical Performance Characteristic

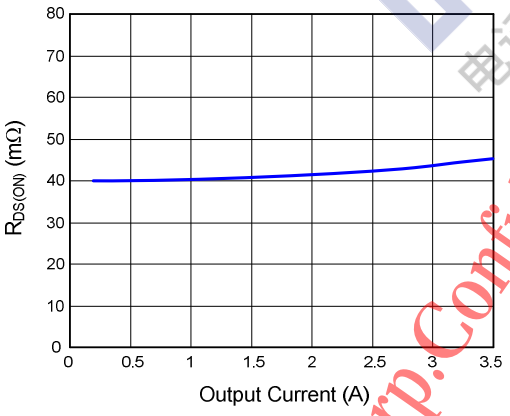
Quiescent Current vs. Input Voltage



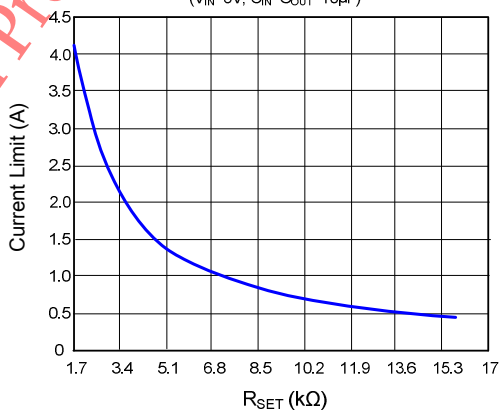
Shutdown Current vs. Input Voltage



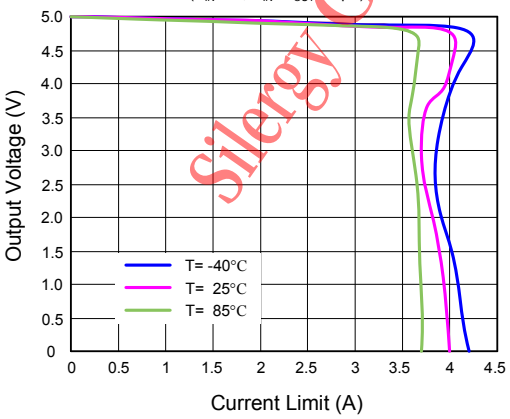
$R_{DS(ON)}$ vs. Output Current
(V_{IN}=5V, C_{IN}=C_{OUT}=10μF)



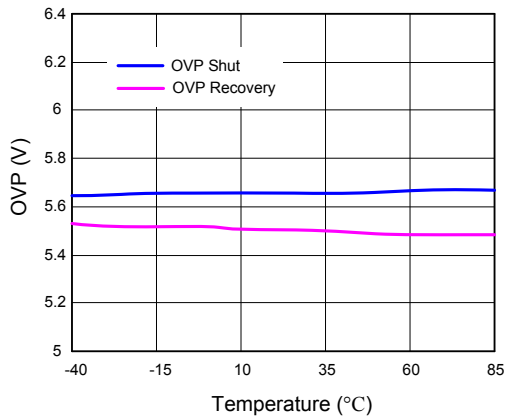
R_{SET} vs. Current Limit
(V_{IN}=5V, C_{IN}=C_{OUT}=10μF)



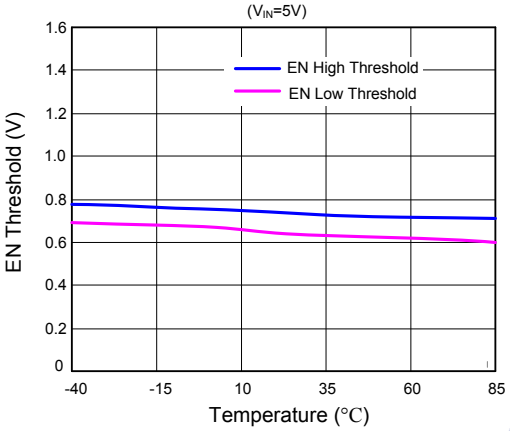
Current Limit vs. Output Voltage
(V_{IN}=5V, C_{IN}=C_{OUT}=10μF)



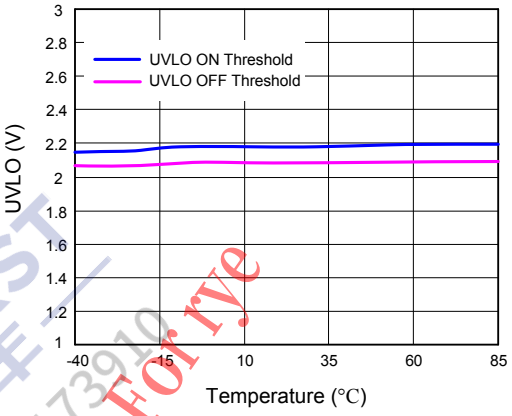
OVP Threshold vs. Temperature



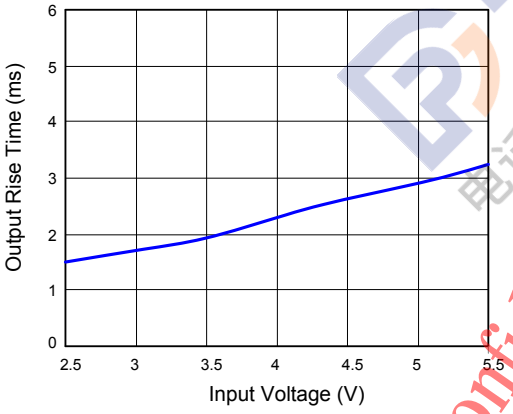
EN Threshold vs. Temperature
(V_{IN}=5V)



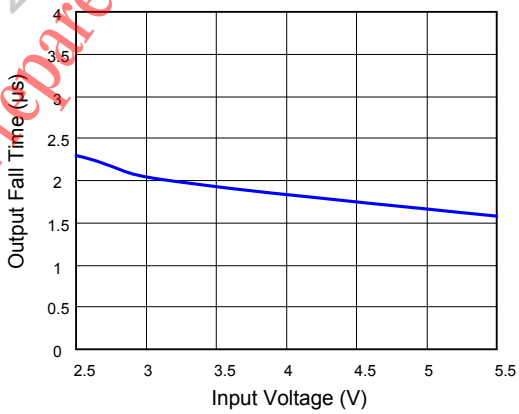
UVLO Threshold vs. Temperature



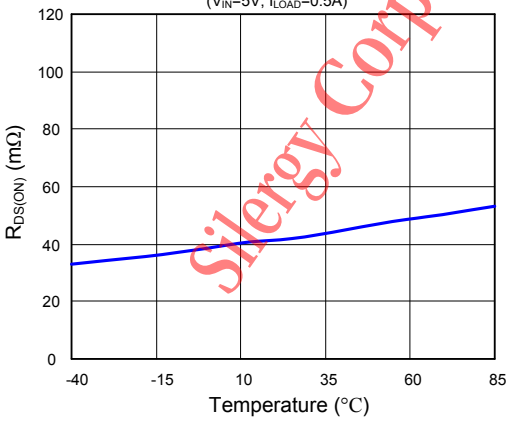
Output Rise Time vs. Input Voltage
(C_{IN}=C_{OUT}=10μF, null load)



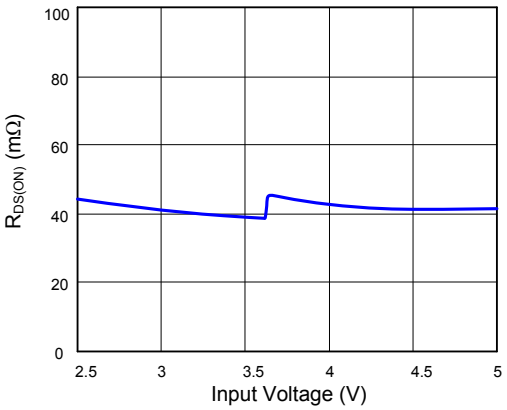
Output Fall Time vs. Input Voltage
(C_{IN}=C_{OUT}=10μF, null load)



$R_{DS(ON)}$ vs. Temperature
(V_{IN}=5V, I_{LOAD}=0.5A)

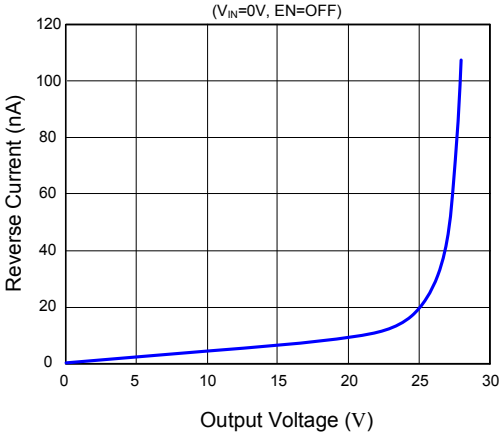


$R_{DS(ON)}$ vs. Input Voltage
(C_{IN}=C_{OUT}=10μF, I_{LOAD}=0.5A)



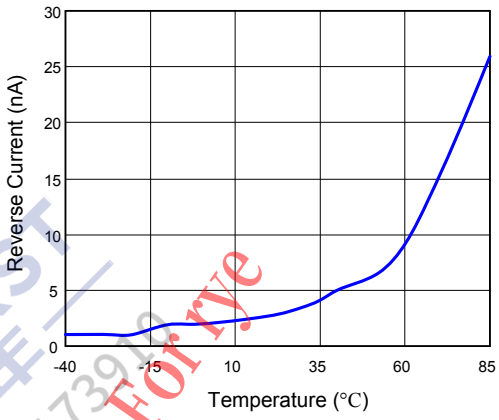
Reverse Current vs. Output Voltage

(V_{IN}=0V, EN=OFF)



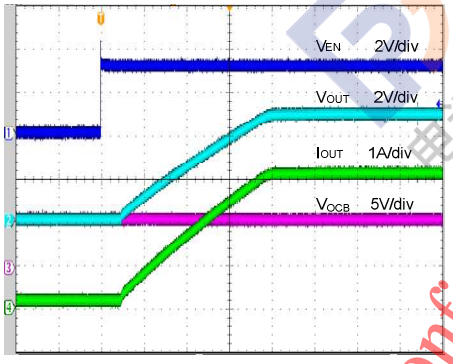
Reverse Current vs. Temperature

(V_{IN}=0V, V_{OUT}=5V, EN OFF)



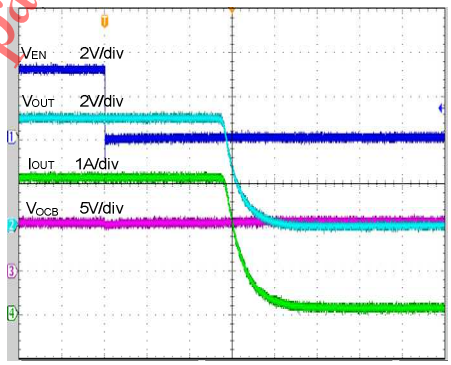
Startup from Enable

(V_{IN}=5V, C_{IN}= C_{OUT}=10μF,1.6Ω Load)



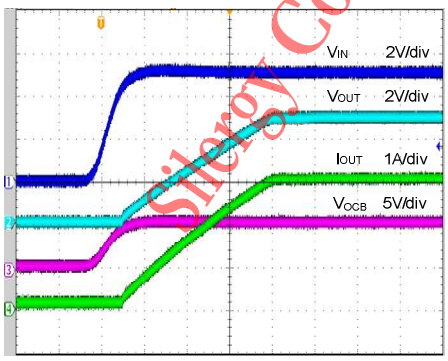
Shutdown from Enable

(V_{IN}=5V, C_{IN}=C_{OUT}=10μF, 1.6Ω Load)



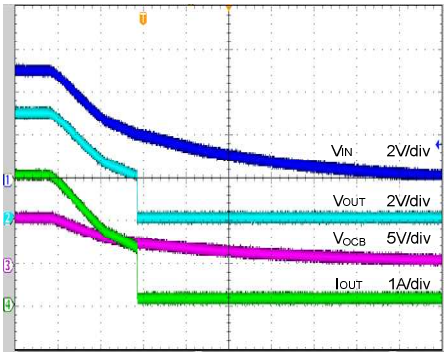
Startup from V_{IN}

(V_{IN}=5V, C_{IN}= C_{OUT}=10μF, 1.6Ω Load)



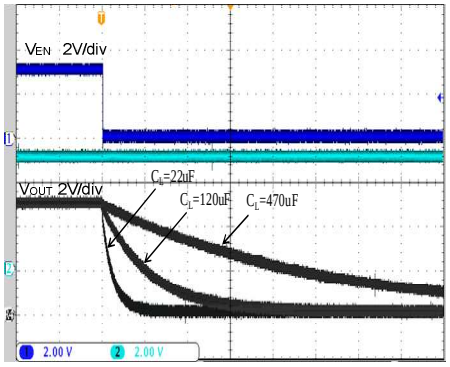
Shutdown from V_{IN}

(V_{IN}=5V, C_{IN}=C_{OUT}=10μF, 1.6Ω Load)



Turn off Delay Time and Fall Time

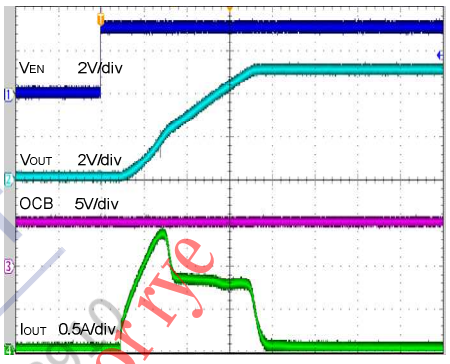
(V_{IN}=5V, R_L=10Ω, C_{IN}=C_{OUT}=10μF)



Time (2ms/div)

Inrush Current with Different Load Capacitance

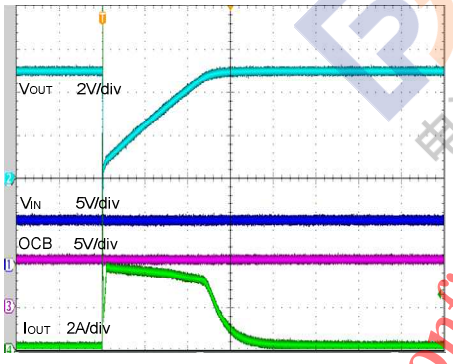
(V_{IN}=5V, C_{IN}=C_{OUT}=10μF, C_L=470uF , R_L=10Ω)



Time (800μs/div)

Capacitance Load Inrush Response

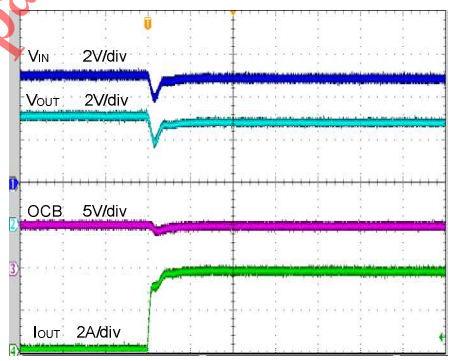
(V_{IN}=5V, C_{IN}=C_{OUT}=10μF, R_L=10Ω , 470μF plug in)



Time (200μs/div)

Resistance Load Inrush Response

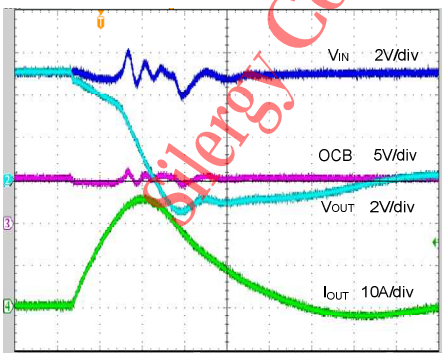
(V_{IN}=5V, C_{IN}=C_{OUT}=10μF, R_L=1.3Ω)



Time (10μs/div)

Short Circuit Response

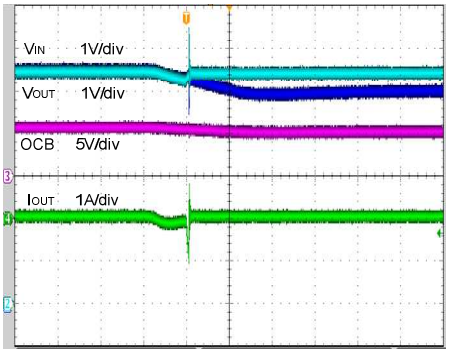
(V_{IN}=5V, C_{IN}=C_{OUT}=10μF)



Time (2μs/div)

Reverse-Voltage Protection Response

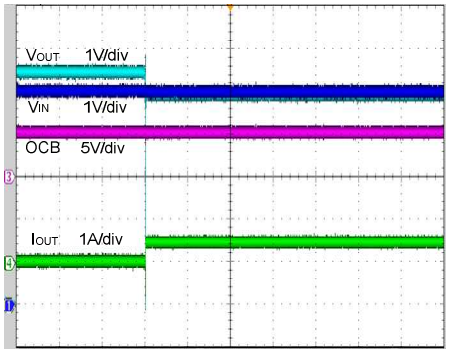
(V_{IN}=5.5V→5V, V_{OUT}=5.5V, C_{IN}=C_{OUT}=10μF)



Time (400μs/div)

Reverse-Voltage Protection Recovery

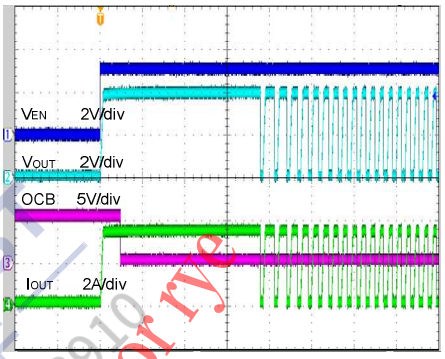
(V_{IN}=5V , C_{IN}=C_{OUT}=10μF, R_L=10Ω, 5.5V V_{OUT} Removed)



Time (200ms/div)

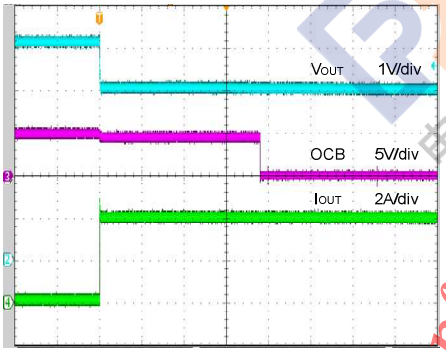
Thermal Shutdown Response

(V_{IN}=5V , C_{IN}=C_{OUT}=10μF, R_L=1.3Ω)



Time (40ms/div)

OCB Response During Over Load



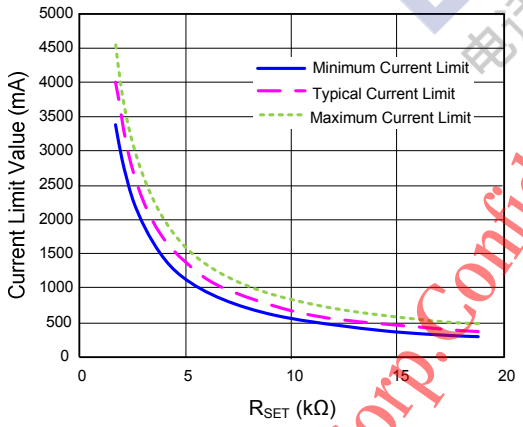
Time (4ms/div)

Operation

The SY6861A1/A2/B1/B2 is a current limited N-channel MOSFET power switch designed for high-side load-switching applications. It incorporates the back to back N-channel MOSFET, so the IC prevents the current-flow from OUT to IN when OUT being externally forced to a higher voltage than IN when the IC is disabled.

Over Current Protection

The SY6861B1/B2 supports current limit programming by connecting a resistor R_{SET} from the ISET pin to ground. The recommended 1% resistor for R_{SET} is 1.878k to 17.8k to ensure stability of internal regulation loop. Many applications require that the minimum current limit is above a certain current level or that the maximum current limit is below a certain current level, so it is important to consider the tolerance of the over current threshold when selecting a value of R_{SET}. The tolerance is showed below:



Minimum current limit: I_{LIM} (A) = 5797/R_{SET} (Ω)-0.026
Typical current limit: I_{LIM} (A) = 6800/R_{SET} (Ω)
Maximum current limit: I_{LIM} (A) = 7640/R_{SET} (Ω)+0.07

The current limit threshold of SY6861A1/A2 is fixed at 3.6A for 3A USB new type C application.

When the over-current condition is sensed, the gate of the pass switch is modulated to achieve constant output current. If the over current condition persists for a long time, the junction temperature may exceed 150°C, and over-temperature protection will shut down the part. Once the chip temperature drops below 130°C, the part will restart.

Fault Flag(OCB)

The OCB output is asserted (active low) when input OVP or thermal shutdown protection is triggered or over current condition persists for 15ms. The output remains asserted until fault condition is removed. Connecting a heavy capacitance load to an enabled device can cause a momentary over current condition. However, no false reporting on OCB occurs due to 15ms deglitch circuit.

Over Voltage Protection

SY6861A1/A2/B1/B2 integrates over voltage protection for the input pin. When the IC is in the ON state and the VIN exceeds 5.6V (typ.), the power FET will be turned off to protect low voltage input stage during the output voltage is higher than 5.6V (typ.). Meanwhile, OCB is pulled low to indicate fault condition. Once the output voltage is lower than the input voltage, the power FET will be turned on and OCB is released to high impedance.

Supply Filter Capacitor

In order to prevent the input voltage drooping during hot-plug events, a 1μF ceramic capacitor from VIN to GND is strongly recommended. However, higher capacitor values could reduce the voltage droop on the input further. Furthermore, an output short will cause ringing on the input without the input capacitor. It could destroy the internal circuitry when the input transient exceeds the absolute maximum supply voltage even for a short duration.

Output Filter Capacitor

A 10μF output ceramic capacitor is recommended to be placed close to the IC and output connector to reduce voltage drop during load transient. Some illegal USB PD device will provide 20V bus voltage without USB negotiation. Therefore the output capacitor should be larger than 4.7μF to decouple the large spike when unstandardized USB PD device plug in. The SY6861A1/A2/B1/B2 is guaranteed to be safe from damage with OUT voltage up to 28V. Nevertheless, voltage transient above 28V may cause permanent damage. A TVS is recommended to clamp the voltage spike.

Reverse block Function:

The SY6861A1/A2/B1/B2 integrates reverse block function. Once the deviation voltage of OUT-IN exceeds 60mV, the reverse block is triggered. The power FET will be shutdown in 600ns to block the reverse current flow from OUT to IN.

PCB Layout Guide

For the best performance of the SY6861A1/A2/B1/B2, the following guidelines must be strictly followed:

1. Keep all VBUS traces as short and wide as possible and use at least 2 ounce copper for all VBUS traces.
2. Locate the output capacitor as close to the connectors as possible to lower the impedance (mainly inductance) between the port and the capacitor to improve transient performance.
3. Input and output capacitors should be placed closed to the IC and connected to ground plane to reduce the noise coupling.

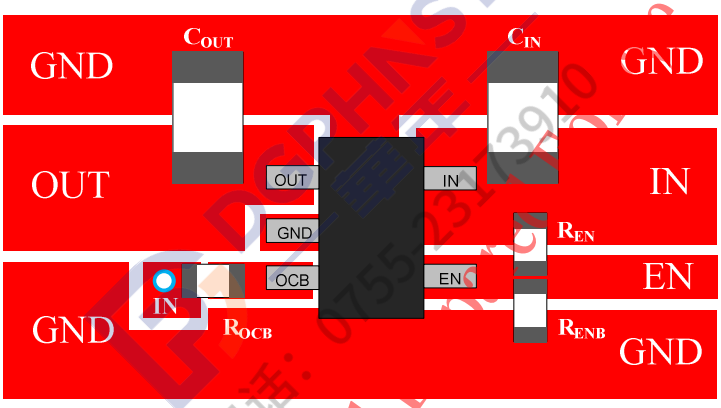


Figure 7. SY6861A1/A2 PCB Layout Suggestion

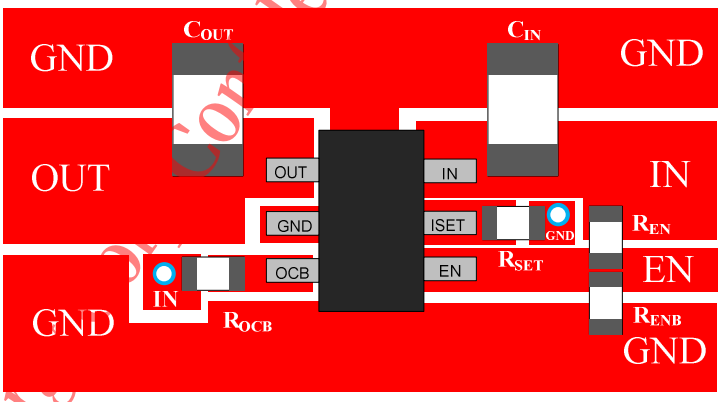
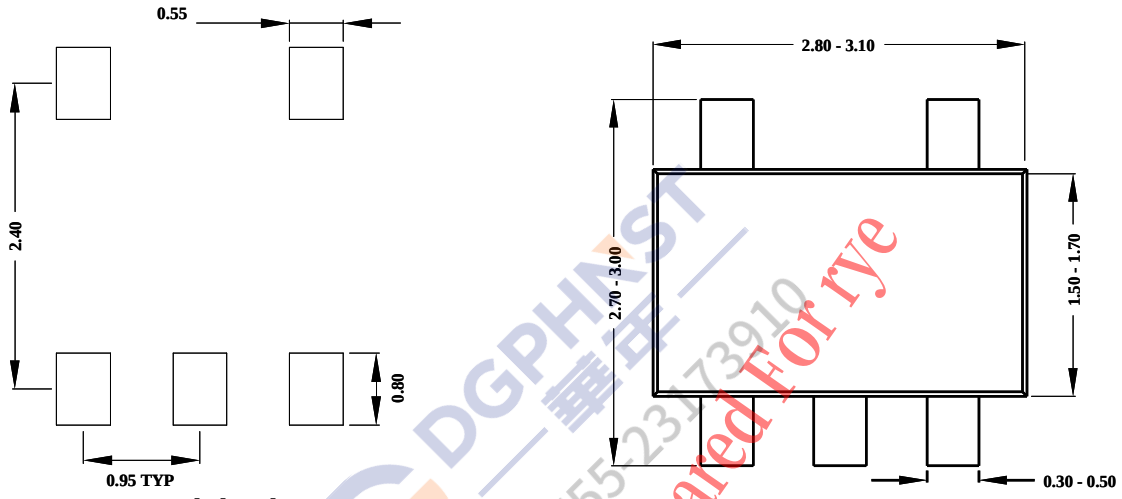
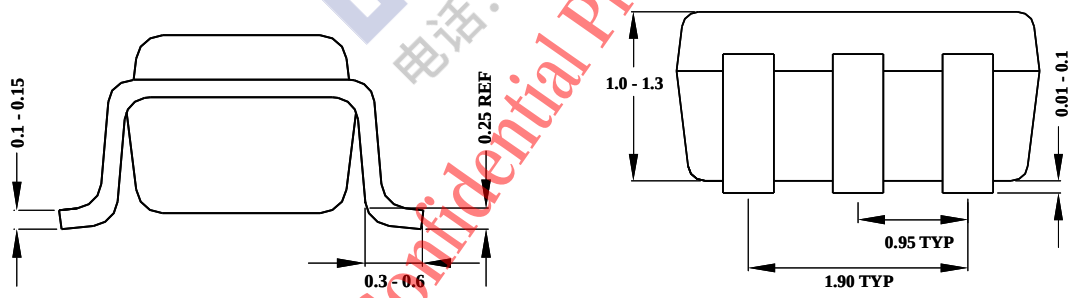


Figure 8. SY6861B1/B2 PCB Layout Suggestion

SOT23-5 Package Outline & PCB Layout Design

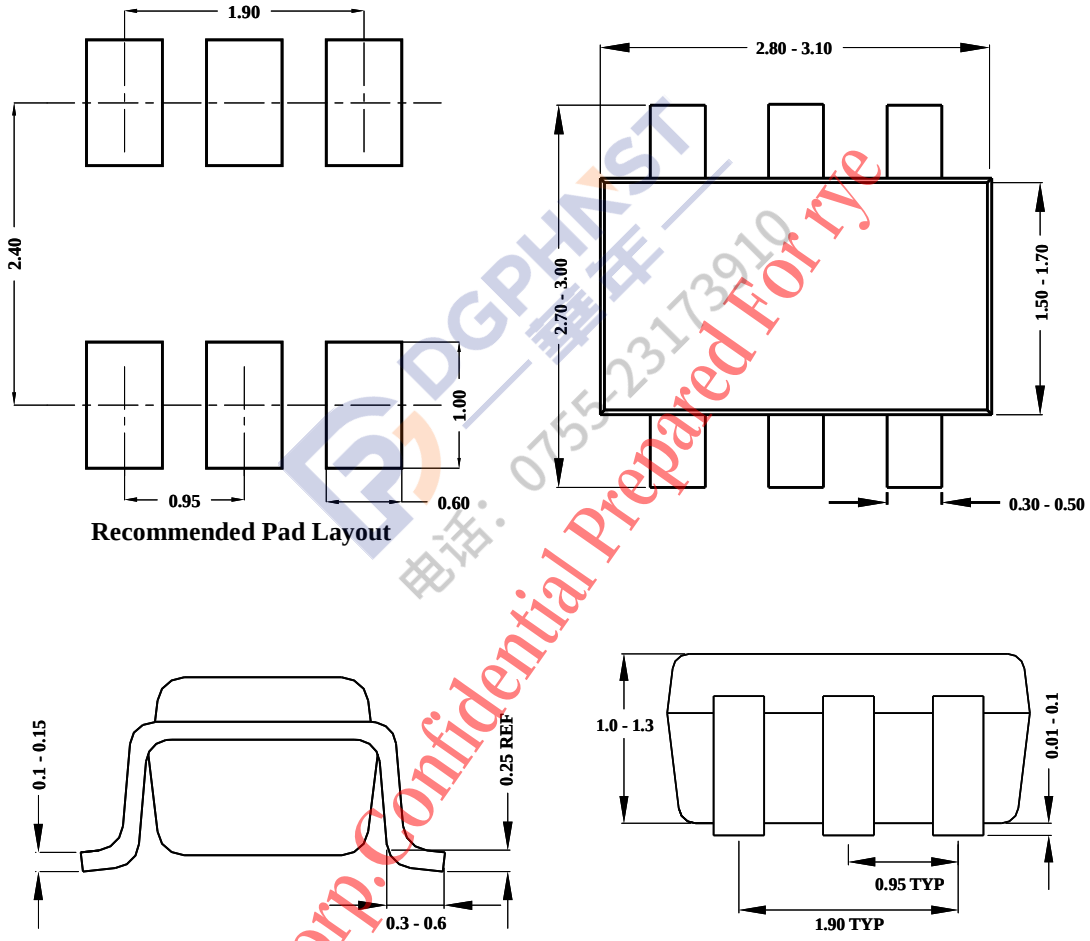


Recommended Pad Layout



Notes: All dimensions are in millimeters.
All dimensions don't include mold flash & metal burr.

SOT23-6 Package Outline & PCB Layout Design



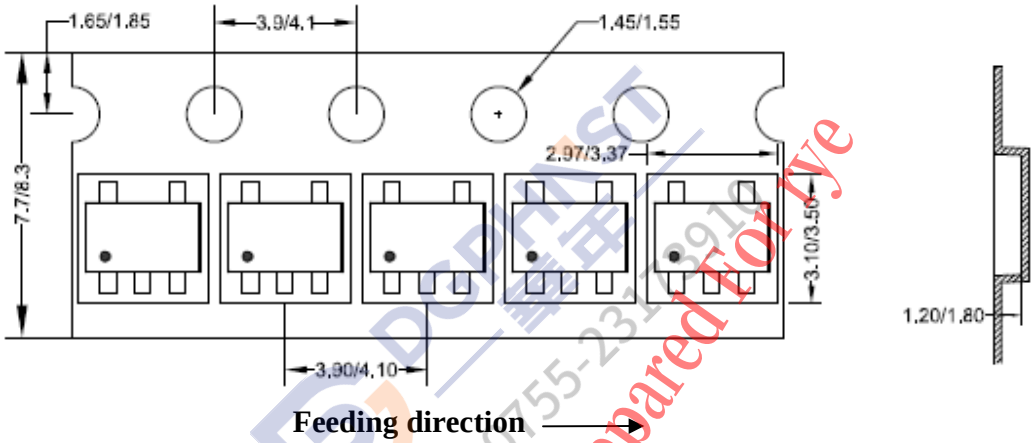
Recommended Pad Layout

Notes: **All dimensions are in millimeters.**
All dimensions don't include mold flash & metal burr.

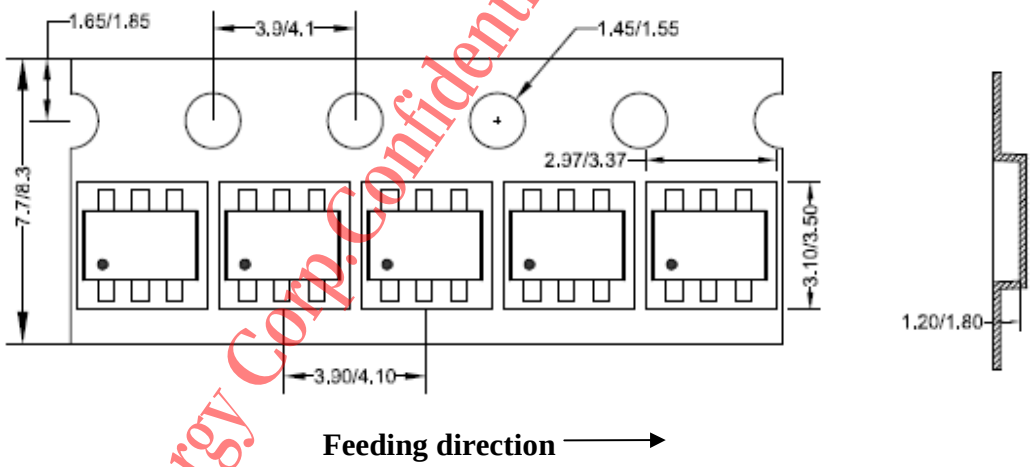
Taping & Reel Specification

1. Taping orientation

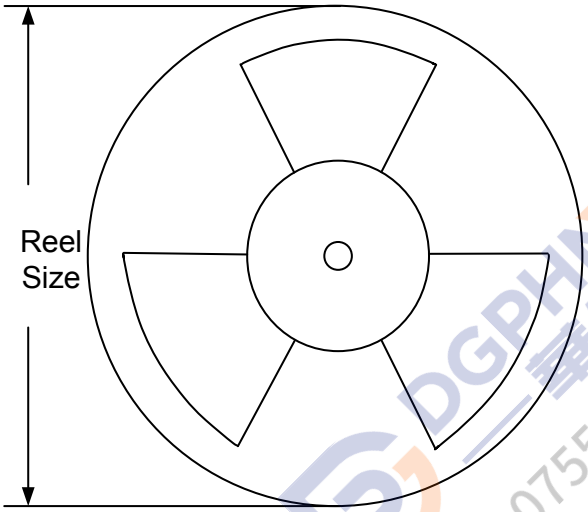
SOT23-5



SOT23-6



2. Carrier Tape & Reel specification for packages



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
SOT23-5	8	4	7"	280	160	3000
SOT23-6	8	4	7"	280	160	3000

3. Others: NA

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